

Lab 5

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Objective-

The objective of this lab was to learn how to use the timer while using the LEDs.

Equipment used-

Software: a text editor and an 8051 ASM assembler

A step debugger that can be used to execute a program one step at a time

Register, code memory, data memory, and input/output port contents are displayed to aid debugging.

Test Results-

Part A light 1 on

The screenshot displays the IAR Embedded Workbench IDE for the 8051 microcontroller. The main window shows the assembly code being executed, with the instruction `setb TR0` highlighted. The register window shows the status of various registers, including the Program Counter (PC) at 8051. The data memory window shows the contents of memory locations. The hardware simulation panel at the bottom shows the state of various components, including a 7-segment display showing the digit '1', a keypad, an ADC, and a motor.

Part A light 2 on

System Clock (MHz) 12.0 | 50000 | Update Freq.

RST Step Run New Load Save Copy Paste

Time: 2s 899ms 708us - Instructions: 1450

```

0024| setb TR0
0026| here2: jnb TF0, here2
0029| clr TR0
002B| clr TF0
002D| dec R5
002E| mov A, R5
002F| JNZ again2
0031| cpl pl.1
0033| mov R5, #60
;jmp function
;cpl pl.2
again3:
0035| mov TL0, #0B0h
0038| mov TH0, #3ch
003B| setb TR0
003D| here3: jnb TF0, here3
    
```

8051

4.94 V output DAC

7 6 5 4 3 2 1 0

8888

ADC 11111111

Motor Enabled

Part A light 3 on

System Clock (MHz) 12.0 | 50000 | Update Freq.

RST Step Run New Load Save Copy Paste

Time: 5s 833ms 953us - Instructions: 2950

```

002F| here1: jnb TF0, here1
0012| clr TR0
0014| clr TF0
0016| dec R5
0017| mov A, R5
0018| JNZ again1
001A| cpl pl.0
001C| mov R5, #30
;jmp function
;cpl pl.1
again2:
001E| mov TL0, #0B0h
0021| mov TH0, #3ch
0024| setb TR0
0026| here2: jnb TF0, here2
0029| clr TR0
    
```

8051

4.85 V output DAC

7 6 5 4 3 2 1 0

8888

ADC 11111111

Motor Enabled

Part A light 1 off

System Clock (MHz) 12.0 50000 Update Freq.

RST Step Run New Load Save Copy Paste

Time: 6s 833ms 851us - Instructions: 3450

```

00F0 here1: jnb TF0, here1
0012 clr TR0
0014 clr TF0
0016 dec R5
0017 mov A, R5
0018 JNZ again1
001A cpl pl.0
001C mov R5, #30
      ;jmp function
      ;cpl pl.1
      again2:
001E mov TL0, #0B0h
0021 mov TH0, #3ch
0024 setb TR0
0026 here2: jnb TF0, here2
002A clr TR0
    
```

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Hardware interface: 4.88 V output, Scope DAC, 7-segment display (8888), 0.0 V input, MAX/MIN Motor Enabled, ADC 11111111.

Part A light 2 off

System Clock (MHz) 12.0 50000 Update Freq.

RST Step Run New Load Save Copy Paste

Time: 8s 333ms 699us - Instructions: 4200

```

0024 setb TR0
0026 here2: jnb TF0, here2
0029 clr TR0
002B clr TF0
002D dec R5
002E mov A, R5
002F JNZ again2
0031 cpl pl.1
0033 mov R5, #60
      ;jmp function
      ;cpl pl.2
      again3:
0035 mov TL0, #0B0h
0038 mov TH0, #3ch
003B setb TR0
003D here3: jnb TF0, here3
    
```

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Hardware interface: 4.92 V output, Scope DAC, 7-segment display (8888), 0.0 V input, MAX/MIN Motor Enabled, ADC 11111111.

Reset

System Clock (MHz) 12.0 | 50000 | Update Freq.

RST Step Run New Load Save Copy Paste

Time: 12s 567ms 817us - Instructions: 635

```

0024 | setb TR0
0026 | here2: jnb TF0, here2
0029 | clr TR0
002B | clr TF0
002D | dec R5
002E | mov A, R5
002F | JNZ again2
0031 | cpl pl.1
0033 | mov R5, #60
           ;jmp function
           ;cpl pl.2
           again3:
0035 | mov TL0, #0B0h
0038 | mov TH0, #3Ch
003B | setb TR0
003D | here3: jnb TF0, here3
    
```

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Hardware Interface: 4.98 V output DAC, 11111111 ADC, Motor Enabled.

Part B light on

System Clock (MHz) 12.0 | 50000 | Update Freq.

RST Step Run New Load Save Copy Paste

Time: 1s 499ms 850us - Instructions: 7500

```

000D | setb Tr0
000F | here1: JNB TF0, here1
0012 | clr TR0
0014 | clr TF0
0016 | dec R5
0017 | mov A, R5
0018 | JNZ again1
001A | cpl pl.6
           next2:
001C | mov R5, #40
           again2:
001E | mov TL0, #0B0h
0021 | mov TH0, #3Ch
0024 | setb Tr0
0026 | here2: JNB TF0, here2
    
```

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Hardware Interface: 3.75 V output DAC, 11111111 ADC, Motor Enabled.

Part B light off

The screenshot displays the EdSim9101 software interface for a microcontroller simulation. The main window is divided into several sections:

- System Settings:** System Clock (MHz) is set to 12.0, and Update Freq. is set to 50000.
- Register Window:** Shows various registers including SBUF, TH0, TL0, R7, B, ACC, R5, PSW, R4, IP, R3, IE, R2, FCON, R1, DPH, R0, DPL, SP, TH1, TL1, R1, and PC. The PC register is highlighted with the value 8051.
- Data Memory Window:** Shows memory addresses from 00 to 70, all containing the value 00.
- Assembly Code Window:** Displays the following code:


```

      000D| setb TF0
      000F| here1: JNB TF0, here1
      0012| clr TR0
      0014| clr TF0
      0016| dec R5
      0017| mov A, R5
      0018| JNZ again1
      001A| cpl pl.6
      next2:
      001C| mov R5, #40
      again2:
      001E| mov TL0, #0B0h
      0021| mov TH0, #3Ch
      0024| setb TR0
      here2:
      0026| JNB TF0, here2
      
```
- Pin Configuration Window:** Lists pins P0.0-P0.7 (Keypad Column 2-0, Keypad Row 3-0), P1.0-P1.7 (LED segments a-g), P2.0-P2.7 (SW 0-7), P3.0-P3.7 (ADC RD, Motor Sensor, Display-select Input, AMN Gate Output, ADC INTR, Motor Control Bit 1/0).
- Hardware Control Panel:** Includes a 7-segment display showing '8888', a 5.0V output DAC, a keyboard, an 8-bit UART @ 4800 Baud (No Parity), and an ADC showing 1111111.

Flow Chart-

Conclusion-

This lab was effective in teaching me how to use the 8051 timer. I learned how to use it in conjunction with the LED lights.

Program-

Part A

```
Org 0h
clr p0.7
mov tmod, #01
;function:
;~~~~~
mov R5, #20
    again1:
        mov TL0, #0B0h
        mov TH0, #3ch
        setb TR0
        here1: jnb Tf0, here1
        clr TR0
        clr TF0
        dec R5
        mov A, R5
        JNZ again1
        cpl p1.0
;~~~~~
mov R5, #30
    again2:
        mov TL0, #0B0h
        mov TH0, #3ch
        setb TR0
        here2: jnb Tf0, here2
        clr TR0
        clr TF0
        dec R5
        mov A, R5
        JNZ again2
        cpl p1.1
;~~~~~
mov R5, #60
    again3:
        mov TL0, #0B0h
        mov TH0, #3ch
        setb TR0
        here3: jnb Tf0, here3
        clr TR0
        clr TF0
        dec R5
        mov A, R5
        JNZ again3
        cpl p1.2
end
```

```
Org 0h
clr p0.7
mov TMOD, #01
next1:
mov R5, #20
again1:
mov TL0, #0B0h
mov TH0, #3Ch
setb Tr0
        here1: JNB TF0, here1
        clr TR0
        clr TF0
        dec R5
        mov A, R5
        JNZ again1
        cpl p1.6
next2:
mov R5, #40
again2:
mov TL0, #0B0h
mov TH0, #3Ch
setb Tr0
        here2:
        JNB TF0, here2
        clr TR0
        clr TF0
        dec R5
        mov A, R5
        JNZ again2
        cpl p1.6
ljmp next1
End
```

Part B