Digital Design Lab
EEN 315

Project 1
Signature Analyzer

Group 2
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November 18, 2013

Abstract

This lab is a four-bit signature analyzer with a shift register and probe. They are commonly used to delay signals, for data conversion, and as arithmetic circuits. They can also be used as counters. The first part of the lab is to design a shift register using flip-flops. The next part is to design a signature analyzer.

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Overview

We were able to implement a four bit signature analyzer from our knowledge of shift registers. We created it from flip-flops, multiplexors, and XOR gates.

Objectives

Design a four bit, bi-directional, serial-in/parallel-out shift register with a direction control. When low, it will shift right. When high, it will shift left. We will use JK FF and minimal other logic.

Equipment

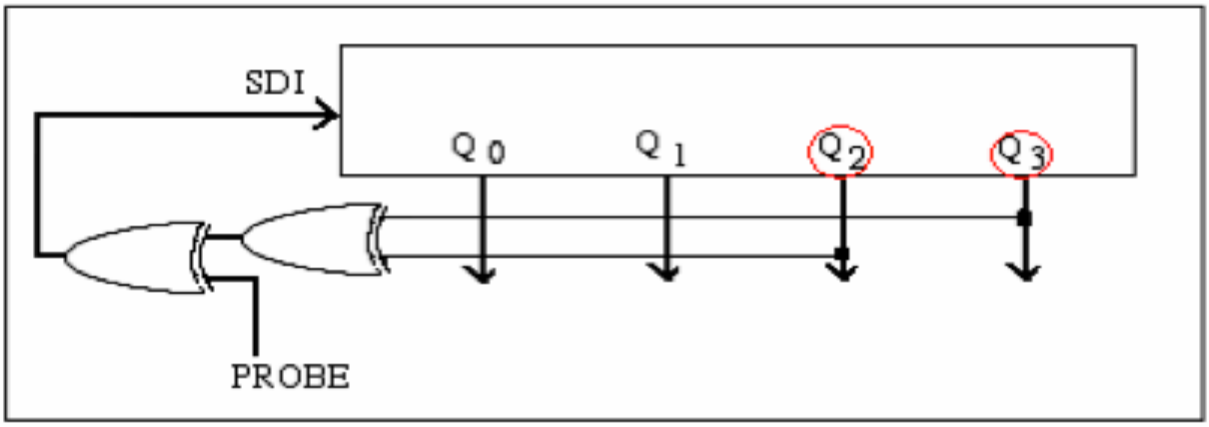
Quartus II software

Description	Quantity
2:1 MUX	8
D Flip Flop	4
XOR gate	2

Description

The first part was to design a four-bit, bi-directional, serial in/ parallel out shift register with a direction control. We did this with four D Flip Flops. We then used four 2:1 multiplexors to decide whether or not to load the given sequence or shift the value. The other four were used to tell it whether to shift left or right. We were able to check this by setting the bits either low or high in the Vector Waveform File in Quartus II.

The next part was to create a probe. This was done by using XOR gates on the two most significant bits, shown below.



We then had to set the given sequences in the Vector Waveform File in the Quartus II software. Once the simulation was complete, we were able to tell if we had implemented the

circuit correctly. We had to try switching or two MSBs and LSBs in order to get it to work. Once we figured out how to properly use the Quartus II software, or problems we were having went away.

Specifications

Line 1: sequence 1010101010
Line 2: sequence 1100110011
Line 3: sequence 1111000011
Line 4: sequence 1111111100
Use JK FF and minimal logic

Design Synthesis

Calculation of steps

Qd	Qc	Qb	Qa	PROBE(INPUT)	Qd+	Qc+	Qb+	Qa+

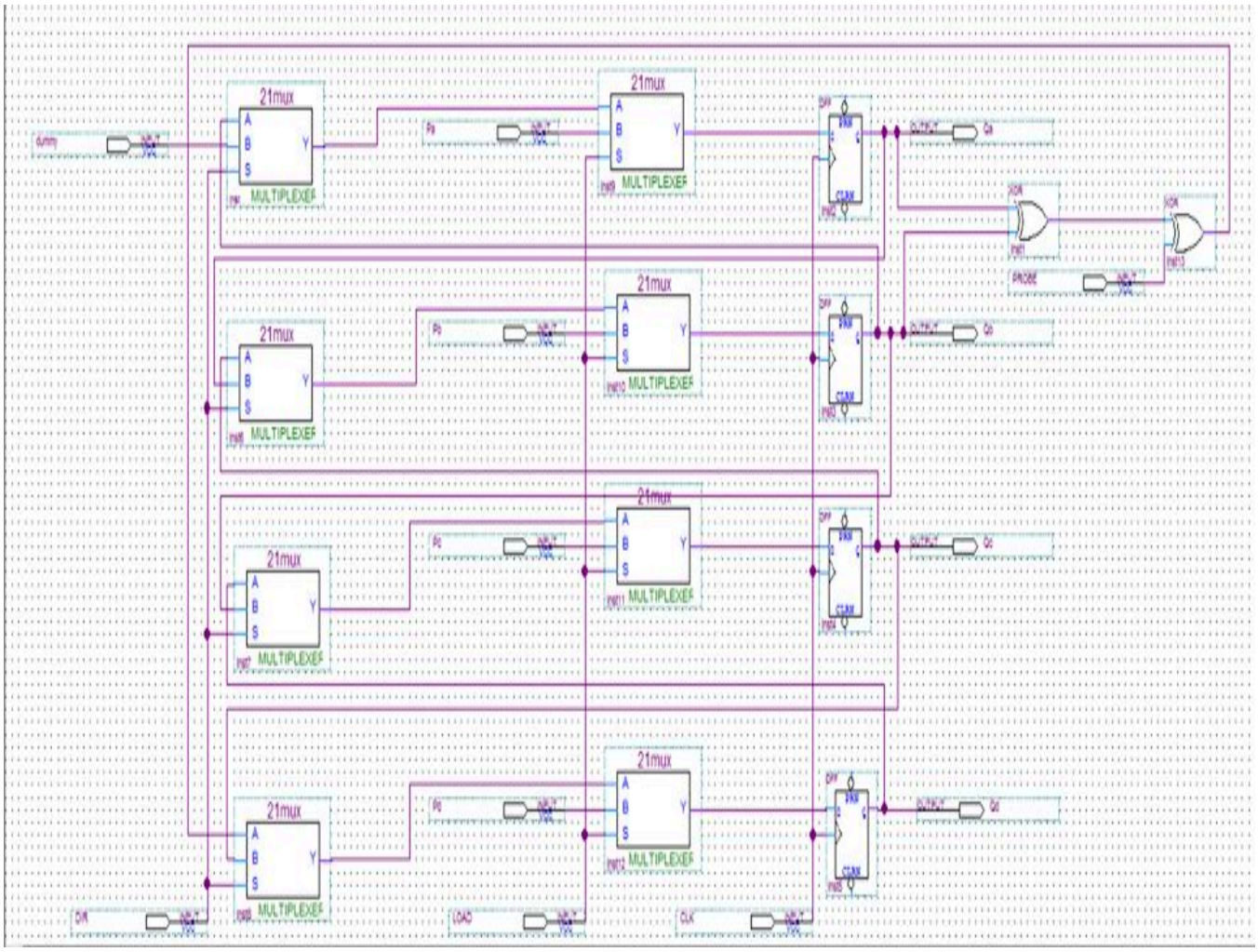
0	0	0	0	1	1	0	0	0
1	0	0	0	0	0	1	0	0
0	1	0	0	1	1	0	1	0
1	0	1	0	0	1	1	0	1
1	1	0	1	1	0	1	1	0
0	1	1	0	0	1	0	1	1
1	0	1	1	1	1	1	0	1
1	1	0	1	0	1	1	1	0
1	1	1	0	1	0	1	1	1
0	1	1	1	0	**0**	**0**	**1**	**1**

Qd	**Qc**	**Qb**	**Qa**	**PROBE(INPUT)**	**Qd+**	**Qc+**	**Qb+**	**Qa+**
0	0	0	0	1	1	0	0	0
1	0	0	0	1	1	1	0	0
1	1	0	0	0	0	1	1	0
0	1	1	0	0	1	0	1	1
1	0	1	1	1	1	1	0	1
1	1	0	1	1	0	1	1	0
0	1	1	0	0	1	0	1	1
1	0	1	1	0	0	1	0	1
0	1	0	1	1	0	0	1	0
0	0	1	0	1	**0**	**0**	**0**	**1**

Qd	**Qc**	**Qb**	**Qa**	**PROBE(INPUT)**	**Qd+**	**Qc+**	**Qb+**	**Qa+**
0	0	0	0	1	1	0	0	0
1	0	0	0	1	1	1	0	0
1	1	0	0	1	1	1	1	0
0	1	1	0	1	0	1	1	1
0	1	1	1	0	0	0	1	1
0	0	1	1	0	0	0	0	1
0	0	0	1	0	1	0	0	0
1	0	0	0	0	0	1	0	0
0	1	0	0	1	1	0	1	0
1	0	1	0	1	**0**	**1**	**0**	**1**

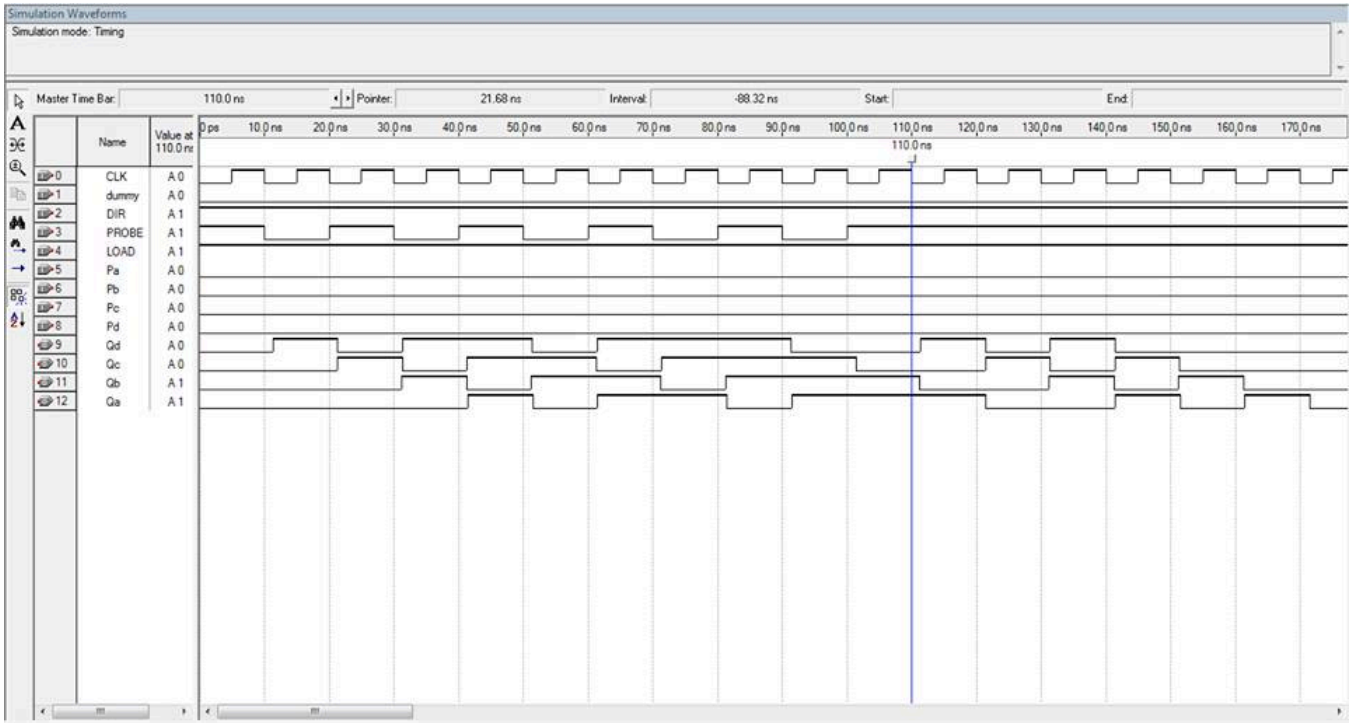
Qd	**Qc**	**Qb**	**Qa**	**PROBE(INPUT)**	**Qd+**	**Qc+**	**Qb+**	**Qa+**
0	0	0	0	1	1	0	0	0
1	0	0	0	1	1	1	0	0
1	1	0	0	1	1	1	1	0
1	1	1	0	1	0	1	1	1
0	1	1	1	1	1	0	1	1
1	0	1	1	1	1	1	0	1
1	1	0	1	1	0	1	1	0
0	1	1	0	1	0	0	1	1
0	0	1	1	0	0	0	0	1
0	0	0	1	0	**1**	**0**	**0**	**0**

Complete Logic Diagram

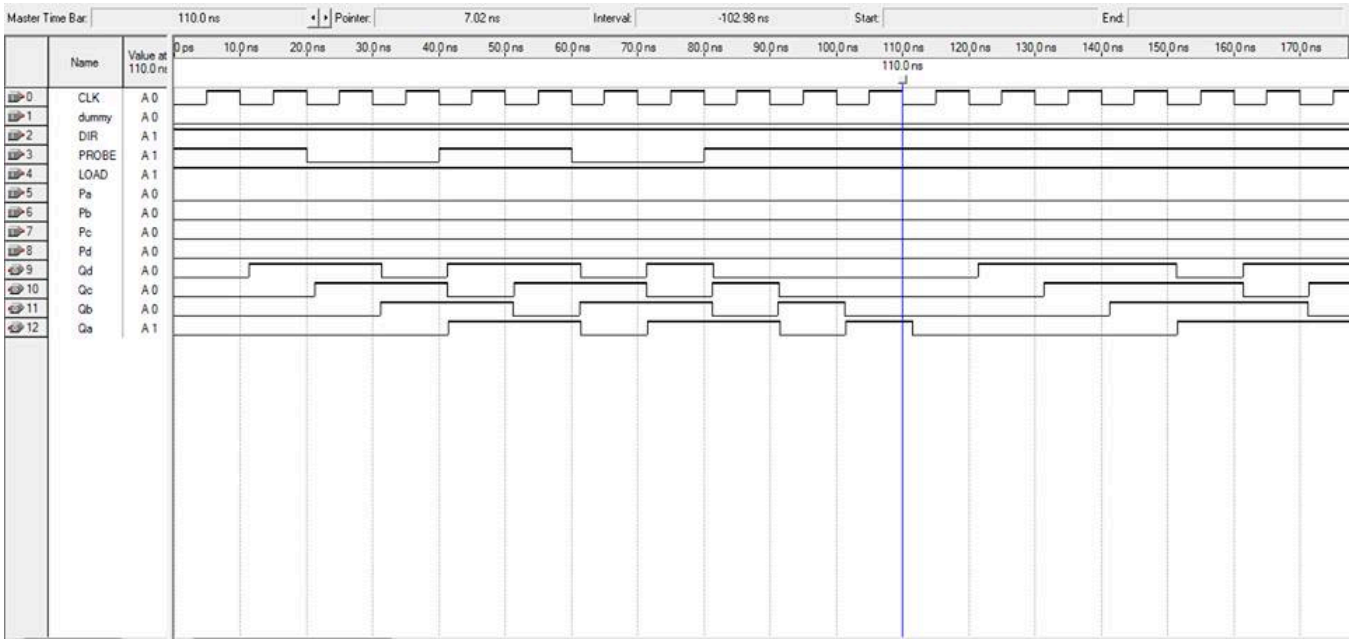


Results and Simulations

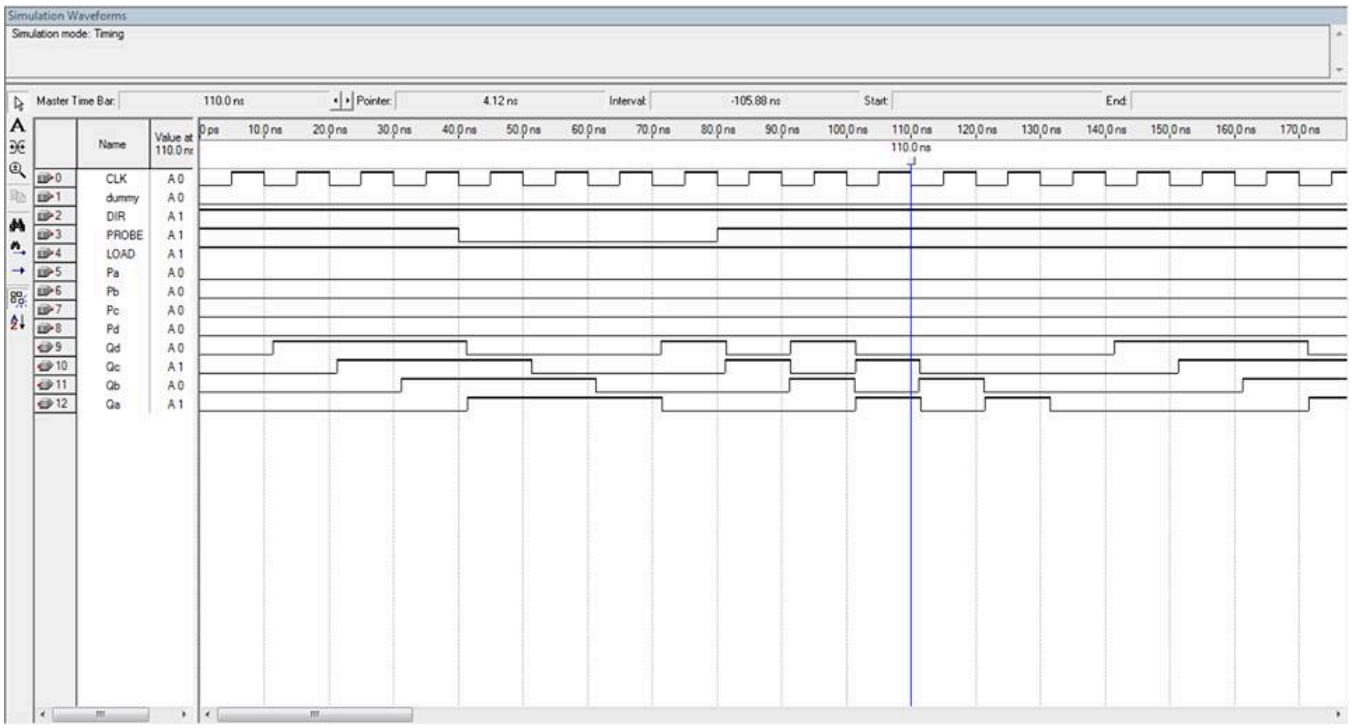
Sequence 1



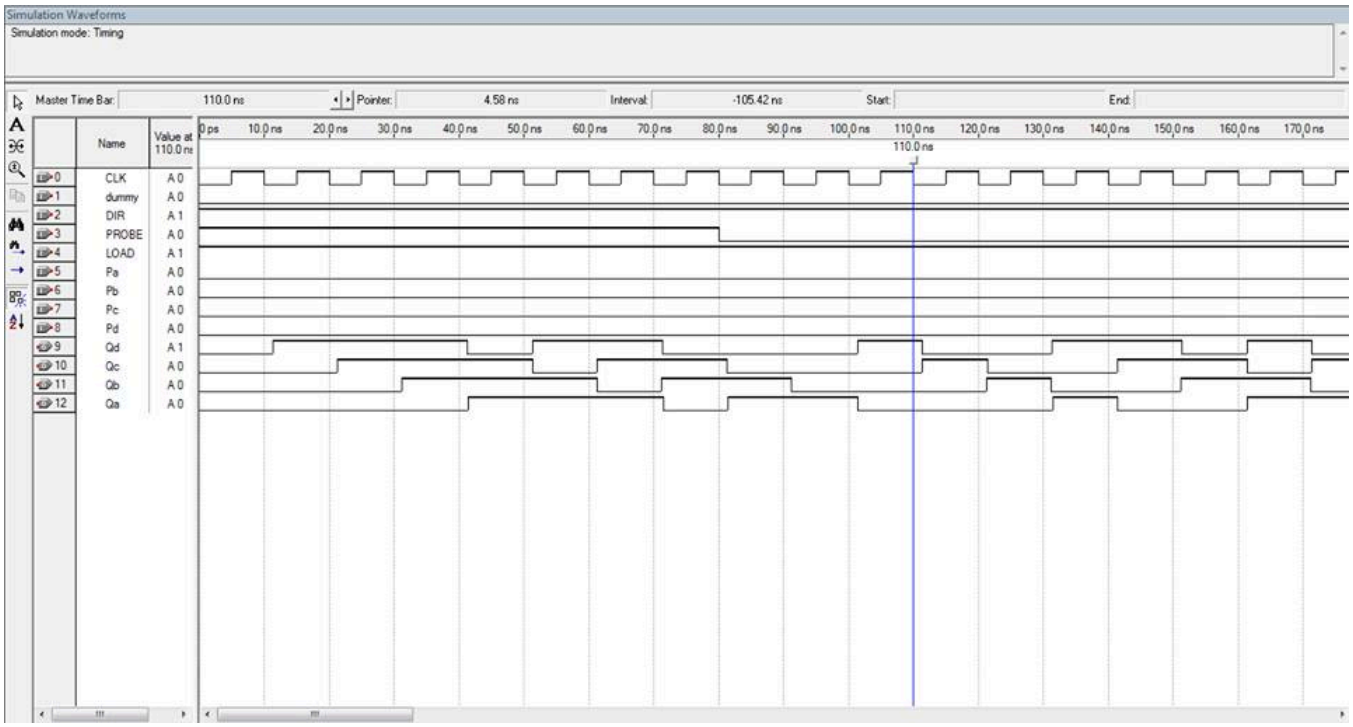
Sequence 2



Sequence 3



Sequence 4



Answers to the questions in the lab handout

none

Conclusion

We successfully implemented the required task of a four bit signature analyzer. Our biggest hurdle to overcome was getting to know the Quartus II software. Once we became familiar with the software, we were able to complete the assignment. We also

Works Cited

none