Digital Design Lab
EEN 315

Lab 1
Title Lab/Project

Group 2
Andrew O'Neil-Smith
(Partner: Austin Cliffton and Amy Zamon)

Sayan Maity, TA

University of Miami

September 23, 2013

Abstract

Part One was to design a 7-segment Display using only LED's and logic gates. In principle, a 7-segment display consists of 7 LED's arranged in the form of digit 8 as shown below. The LEDs are marked as (starting from the top and going clockwise) a, b, c, d, e, f, g.

Part two was to design a state machine that has a single input line X and a single output line Z.
The machine detects the input sequence 101 by producing Z=1 as the last 1 occurs, Z = 0 otherwise. Overlap is allowed.

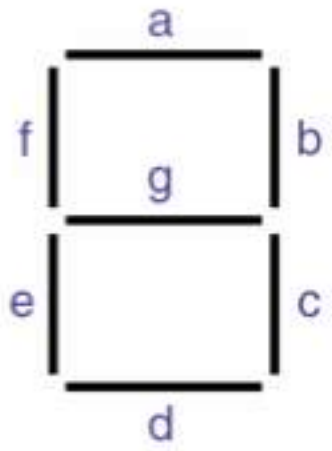
Part three was to connect the two circuits so that when the output of the sequence detector is 1, 1 should show on the seven-segment display; otherwise, 0 should be displayed. Overlapping is okay. Should be completed with D Flip-Flops and NAND gates.

The key results were that we got a seven-segment display to properly display the numbers 0-9. We also got great results on the sequence detector.

The goal was to get familiar with the equipment we will be using this semester.

Table of Contents

Overview



The seven-segment display is a widely used logic circuit (ovens, clocks, etc). Each segment has a letter assigned to it (see figure). Each LED must be connected to ground and a signal through a resistor. The D Flip-Flop senses the sequence “101” and will display a “1” if detected. If not detected, a “0” will be displayed on the seven segment display. Understanding Boolean Logic and Algebra is key to knowing how to do this lab.

Objectives

The objective was to build a seven-segment display using only NAND gates, as well as a sequence detector detecting the sequence “101.”

Equipment

Description	Chip Number
Quad 2---Input NAND gates	7400
Triple 3 Input NAND gates	7410
Quad 4 Input NAND gates	7420
Dual Positive Edge-Triggered D FF	7474

Description

Step one was to make a Truth Table for the seven-segment display. It has four X inputs and seven Letter outputs. The next step was to make K-Maps based on the Truth Table. We solved each K-Map and we realized the equations of Prime Implicants for the display. We then began to make each prime implicant on the breadboard with the NAND gates. Each integrated circuit had to be sent power and ground.

The sequence detector started with the State-Machine, followed by the next state table. We got the input requirements for detecting “101” from that. Then we used K-Maps to figure out the D Flip-Flop formulas. The clock was given manually via the buttons on the test bench.

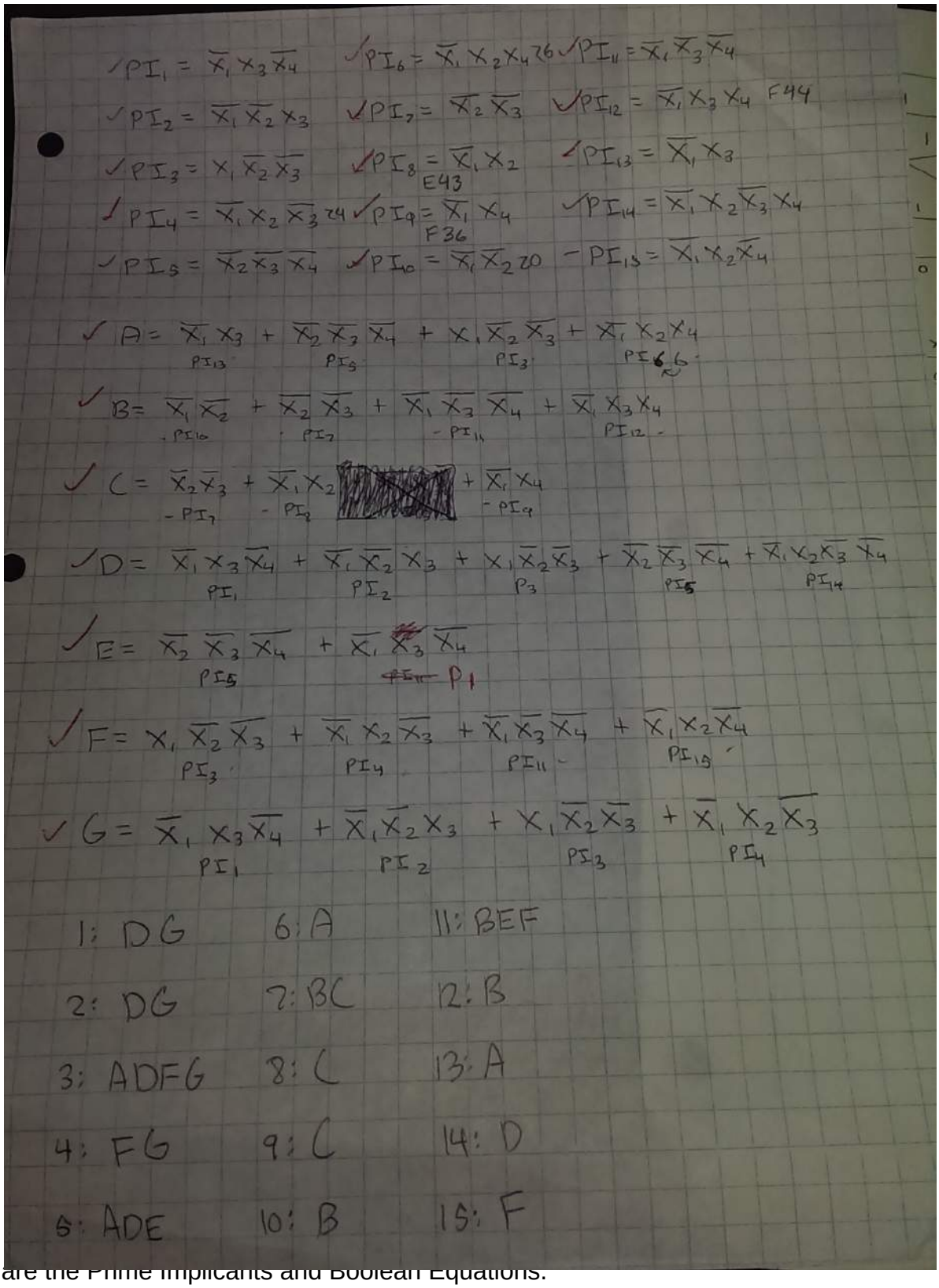
Specifications

Use only NAND gates for the 7 segment display. The sequence detector will use only NAND gates and one D Flip-Flop.

Design Synthesis

Truth Table

N	X1	X2	X3	X4	A	B	C	D	E	F	G
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1
10	1	0	1	0	0	0	0	0	0	0	0
11	1	0	1	1	0	0	0	0	0	0	0
12	1	1	0	0	0	0	0	0	0	0	0
13	1	1	0	1	0	0	0	0	0	0	0
14	1	1	1	0	0	0	0	0	0	0	0
15	1	1	1	1	0	0	0	0	0	0	0



These are the Prime Implicants and Boolean Equations.

K-Maps

A

x1x2	1	0	0	1
x3x4	0	1	0	1
	1	1	0	0
	1	1	0	0

B

x1x2	1	1	0	1
x3x4	1	0	0	1
	1	1	0	0
	1	0	0	0

C

x1x2				
x3x4	1	1	0	1
	1	1	0	1
	1	1	0	0
	0	1	0	0

D

x1x2				
x3x4	1	0	0	1
	0	1	0	1
	1	0	0	0
	1	1	0	0

E

x1x2				
x3x4	1	0	0	1
	0	0	0	0
	0	0	0	0
	1	1	0	0

F

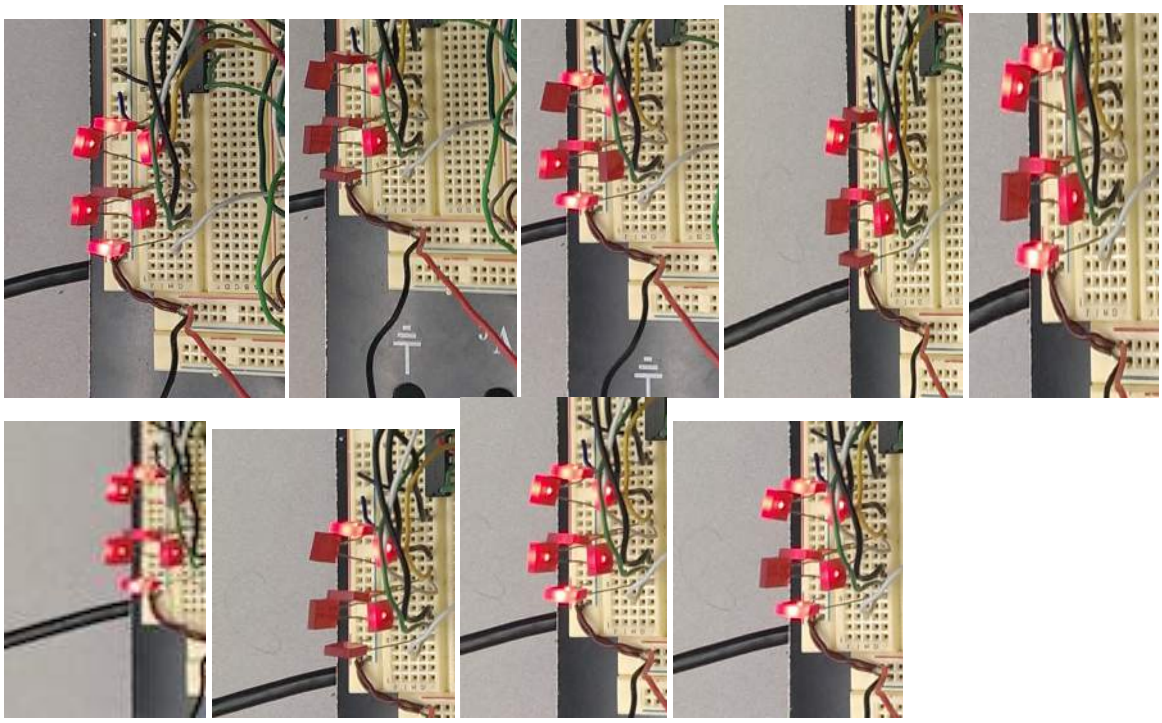
x1x2				
x3x4	1	1	0	1
	0	1	0	1
	0	0	0	0
	0	1	0	0

G

x1x2				
x3x4	0	1	0	1
	0	1	0	1
	1	0	0	0
	1	1	0	0

Complete Logic Diagram

Results and Simulations



1 through 9

Answers to the questions in the lab handout

1.

2. One other use is the transmission of music control data in MIDI (Music Instrument Digital Interface). The sequence detector senses when note “on” and “off’ events occur. It is constantly trying to read a stream of messages.

Conclusion

The project had us create a seven-segment display and a sequence detector using NAND gates. The hardest part of the design was finding time that we could all work on it. It was a challenge to all work equal amounts on it. Our final design could have been neater in terms of wire lengths. I have learned how to get a seven-segment display to work using only NAND gates. I have also learned how to implement a sequence detector.

Works Cited

None